## (12) UK Patent Application (19) GB (11) 2 298 657 (13) A

(43) Date of A Publication 11.09.1996

- (21) Application No 9604614.9
- (22) Date of Filing 04.03.1996
- (30) Priority Data (31) 95004447
- (32) 04.03.1995
- (33) KR

(71) Applicant(s)

Hyundai Electronics Industries Co. Ltd.

(Incorporated in the Republic of Korea)

San 136-1,Ami-ri, Bubai-eub, Ichon-kun, Kyoungki-do 467-860, Republic of Korea

(72) Inventor(s)

Gyung-su Cho

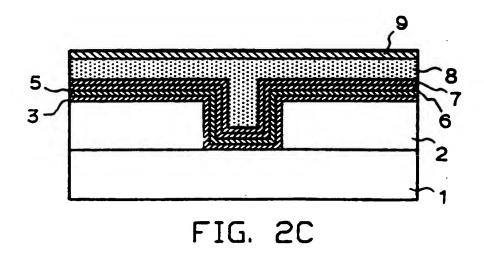
(74) Agent and/or Address for Service

A A Thornton & Co Northumberland House, 303-306 High Holborn, LONDON, WC1V 7LE, United Kingdom

- (51) INT CL<sup>6</sup>
  C23C 16/56 16/34 // H01L 21/768
- (56) Documents Cited EP 0525637 A1 EP 0514103 A1 EP 0209654 A2 US 5136362 A
- (58) Field of Search
  UK CL (Edition O.) C7F FACE FACX FAHE FAHX FAXE
  FAXX FHB FHE FHX , H1K KHAAB KHAAX KHABX
  KHAD
  INT CL<sup>8</sup> C23C 14/06 14/58 16/34 16/56 , H01L 21/285
  Online: WPI, CLAIMS

#### (54) Forming metal interconnects with phase transformed titanium nitride layers

(57) A method of forming metal interconnects for semiconductor devices capable of enhancing yield and reliability comprises first forming a contact hole at a predetermined portion of semiconductor substrate which active regions are formed in and then insulating layer is formed on. Afterwards, titanium and titanium nitride layers, each having a predetermined thickness, are orderly deposited on the contact hole and the insulating layer by Chemical Vapor Deposition. Next, thermal annealing is performed in an atmosphere of nitrogen, in order to change the phase of the deposited Titanium Nitride layer, and the content of N<sub>2</sub> in each layer transformed. Lastly, the metal interconnect is formed to connect the active regions to each other by depositing a interconnecting metal having low resistivity on the diffusion barrier layers and afterward patterning of all layers formed on the contact hole and insulating layer till now. Alternately, it is also possible that the present invention further comprises a step for depositing an arc-thin film which prevents the reflection of light on the interconnecting metal before the patterning of the formed layers occurs. Fig 2C illustrates an assembly in which three phase transformed titanium nitride layers 5, 6, 7 are formed.



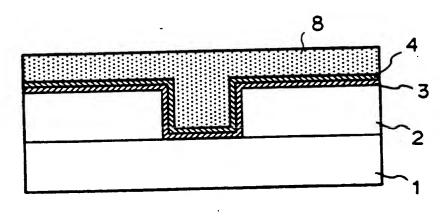


FIG. 1

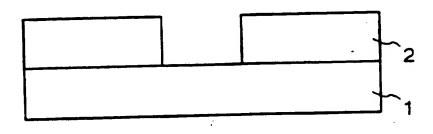
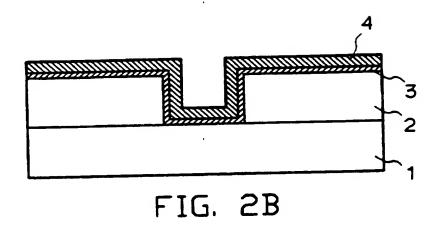
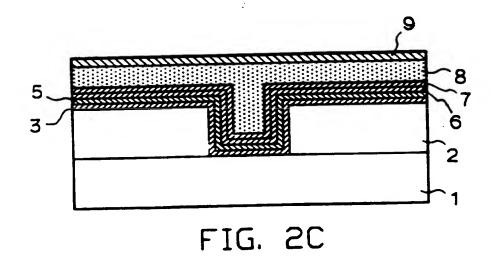
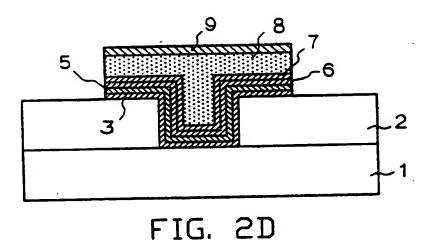


FIG. 2A







### 2298657

# METHODS OF FORMING METAL INTERCONNECTS IN SEMICONDUCTOR DEVICES

#### FIELD OF THE INVENTION

Ē

The present invention relates to a method of forming a semiconductor device, and more particularly to a method of forming a metal interconnect in a semiconductor device including a diffusion barrier metal layer.

10

15

#### DESCRIPTION OF THE PRIOR ART

As the integration of semiconductor device is increased, many methods have been studied to make the interconnect design free and easy, and to make the designation of resistance and current capacitance variable.

In general, aluminum is widely used as the material for metal interconnect of semiconductor device. As the integration is increased, the width of the interconnect is fine, so the current density is increased. The increase of the current density, however, generates failure due to electromigration, anti-reflection and movement of stress, which results in a drop in the reliability. To solve the above problem, a method that deposits copper(Cu) or titanium(Ti) on the interconnect of aluminum(Al) has been provided, but it leads to serious problems such as the failure of insulator and a short of interconnects due to

phenomena such as hillock and whisker.

15

20

Fig. 1 a sectional view of semiconductor device forming the metal interconnect after the formation of the diffusion barrier layer according to an embodiment of the conventional art. In the conventional method, insulating layer 2 is first formed on a semiconductor substrate 1. Afterwards, contact holes are formed at the predetermined portions of the semiconductor substrate 1 by etching some portions of the insulating layer till the surface of the substrate 1 is exposed. Next, diffusion barrier layers of titanium(Ti) 3 and titanium nitride(TiN) 4 are orderly formed by Physical Vapor Deposition. Lastly, metal interconnect 8 using aluminum metal or aluminum alloy is formed on the Titanium Nitride layer 4.

Currently, however, as high integration of device proceeds, the size of the contact hole is more and more decreased. In proportion to the decrease of the contact hole size, the aspect ratio of the contact hole is increased. Accordingly, in a case where the diffusion barrier layers are formed by Physical Vapor Deposition as above, the step coverage is decreased resulting in the diffusion barrier layer being deposited unevenly. Moreover, in a case where the thickness of the barrier layer is increased, a shadow effect is generated at the. corner of the upper portion of the contact hole, making it impossible for the succeeding process to proceed. addition, in a case where the Chemical Vapor Deposition method, in which  $TiCl_4$  reacts on  $NH_3$ , is used to enhance

the step coverage, there is a problem in the excess generation of particles. Therefore, the result is a drop in the yield and reliability of the devices. Furthermore, in this case, there is a problem in reducing the speed of the device because the inner resistance of it is increased by the phase transformation to the amorphous phase during the deposition of TiN.

#### SUMMARY OF THE INVENTION

10

15

23

25

Accordingly, the object of the present invention is to provide a method of forming the metal interconnect of semiconductor device, which can enhance the yield and reliability of a semiconductor device by increasing the step coverage of the diffusion barrier layer and decreasing the inner resistance and the particle generation thereof.

To accomplish the object of the invention, first contact hole is formed at the predetermined portion of semiconductor substrate which active regions are formed in and then insulating layer is formed on. Afterwards, Titanium and Titanium Nitride layers each having a predetermined thickness are orderly deposited on the contact hole and the insulating layer by Chemical Vapor Deposition. Next, thermal annealing is performed in an atmosphere of nitrogen, in order to change the phase of the deposited Titanium Nitride layer and the content of N2 in each layer transformed. Lastly, the metal interconnect is formed to

connect the active regions to each other by depositing a interconnecting metal having low resistivity on the diffusion barrier layers and afterwards, patterning of all layers is formed on the contact hole and insulating layer.

3

20

Alternatively, it is also possible that the present invention further comprises of a step for depositing an arc-thin film which prevents the reflection of light on the interconnecting metal before the patterning of the formed layers occurs.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a sectional view for illustrating a method

of forming the metal interconnect according to the

conventional embodiment.

Figs. 2A to 2D are sectional views, showing sequential processes of forming the metal interconnect, according to an embodiment of the present invention, respectively.

#### DETAILED DESCRIPTION OF THE PRESENT INVENTION

Hereinbelow, a preferred embodiment of the present invention is illustrated referring to Figs. 2A to 2D.

Figs. 2A TO 2D are sectional views showing sequential processes for forming a metal interconnect according to an embodiment of the present invention.

First, referring to Fig. 2A, an insulating layer 2 is deposited on a semiconductor substrate 1 including active formed at is then hole contact predetermined portion of the insulating 2 layer etches the which method photolithographic insulating layer till the surface of the semiconductor Then, as shown in Fig. 2B, a substrate 1 is exposed. Titanium layer 3 is deposited on the inner portion of the contact hole and the whole surface of the insulating layer 2. The Titanium layer 3 is very thinly formed to a degree capable of maintaining the shape of the contact hole 2 by Chemical Vapor Deposition which react TiCl4 with NH3 or The Chemical Vapor Deposition method is to enhance the step coverage of the inside of the contact hole. Then, a Titanium Nitride layer 4 is formed on the Titanium layer The Titanium Nitride layer 4 is formed by Chemical Deposition to depress the generation of In other words, the method uses the raw particles. tetradimethyl-aminotitanium only of material  $\label{eq:timescale} \mbox{[Ti}\{N\left(CH_{3}\right)_{2}\}_{4}\mbox{] or tetradiethylaminotitanium }\mbox{[Ti}\{N\left(C_{2}H_{5}\right)_{4}\}\mbox{],}$ and decomposes Titanium Nitride from one of said two compounds by thermal annealing wherein, the supplied gas is Nitrogen and/or Helium. The deposition temperature of the TiN ranges from 300 to 500 °C and the pressure of the furnace is controlled to the range from 5 to 10 mTorr. What is formed is an amorphous layer. Afterwards, the semiconductor substrate which the above layers were formed on, is thermally annealed in an atmosphere of nitrogen for the temperature

20

range of 400 to 600 °C. Through the annealing process, the titanium nitride layer 4 is transformed to three titanium nitride layers 5, 6, 7 whose physical properties are different from one another. The lower or first layer is composed of titanium nitride 5 that exists as an amorphous layer, the middle or second layer is composed of titanium nitride 6 that exists as a crystalline layer, and the upper or third layer is composed of titanium nitride 7 that exists as a nitrogen-rich crystalline layer. the Rapid Thermal Annealing (RTA) method can also be used on behalf of the conventional thermal annealing. performed at the temperature range of 700 to 900°C and in the time range of 10 to 30 seconds. Titanium nitride 4 of single layer has very high resistance because it is in an amorphous state, but the triple layer of titanium nitride 5,6,7 has a low resistance compared with the single layer titanium nitride 4 because its physical properties are different from one another. The titanium layer 3 and titanium nitride layers 5, 6, 7 act as diffusion barrier metal for preventing the diffusion of metal atoms which would occur without the existence of the barrier. Afterwards, as shown in Fig. 2C, a interconnecting metal such as aluminum, copper, or alloy of aluminum and copper etc., is formed on the diffusion barrier layer, wherein the interconnecting metal connects the active regions to other by depositing any metal having resistivity on the diffusion barrier layers. Afterwards,

15

an arc-metal layer 9 is formed on the metal layer 8 by Chemical Vapor Deposition. Here, the arc-metal layer is to prevent the light from reflecting on the interconnecting metal when light is exposed performed to form a pattern of the metal interconnect. The arc-thin film is composed of tetradimethylaminotitanium or tetradiethylaminotitanium, and the range of the deposition temperature is from 300 to 450°C. The step for forming the arc-thin film 9 can be deleted according to each case.

Lastly, as shown in Fig. 2D, the metal interconnect is formed by patterning said metal layers 3, 5, 6, 7, 8, 9. The metal layer 8 can be substituted for a metal having high conductivity such as Tungsten.

13

15

As previously described in detail, the present invention can reduce the resistance of titanium nitride and the generation of particles, and enhance the step coverage by transforming titanium nitride of a single layer to titanium nitride of three layers three layers are formed individual properties. The through a method that consists of forming titanium nitride by thermal decomposition of the raw material including nitrogen and titanium, and annealing the deposited titanium nitride in an atmosphere of nitrogen. Accordingly, it provides effects enhancing not only the reliability and yield but also the speed of the signal transfer.

Other features, advantages and embodiments of the invention disclosed herein will be readily apparent to those exercising ordinary skill after reading the

foregoing disclosures. In this regard, while specific embodiments of the invention have been described in considerable detail, variations and modifications of these embodiments can be effected without departing from the spirit and scope of the invention as described and claimed.

#### WHAT IS CLAIMED IS:

10

15

15

1. A method of forming a metal interconnect for semiconductor devices comprising the steps of:

forming a contact hole at a predetermined portion of a semiconductor substrate on which an insulating layer is formed;

depositing titanium and titanium nitride layers, each having a predetermined thickness, on said insulating layer said contact hole in an order by Chemical Vapor Deposition;

thermally annealing said substrate in an atmosphere of nitrogen wherein said titanium nitride layer is phase-transformed to titanium nitride layers which each layers has other nitrogen

depositing a metal layer having low resistivity on the titanium nitride layer; and

patterning the layers formed on the contact hole and insulating layer till now.

- 2. The method in accordance with claim 1, wherein said titanium is formed by chemical vapor deposition which reacts TiCl $_4$  with NH $_3$ .
- 3. The method in accordance with claim 1, wherein said titanium nitride is formed by thermal decomposition of Tetradimethylaminotitanium.

4. The method in accordance with claim 1, wherein said titanium nitride is formed by thermal decomposition of Tetradiethylaminotitanium.

- 5. The method in accordance with claim 3, wherein said thermal decomposition is performed at a condition of temperature of 300 to 500 °C, pressure of 5 to 10 mTorr.
- 6. The method in accordance with claim 4, wherein said thermal decomposition is performed at a condition, of temperature of 300 to 500 °C, pressure of 5 to 10 mTorr.
- 7. The method in accordance with claim 1, wherein said
  thermal annealing for phase transformation of titanium
  nitride is performed in an atmosphere of nitrogen and
  temperature of 400 to 600°C for 30 to 60 minutes.
- 8. The method in accordance with claim 1, wherein said thermal annealing for phase transformation of titanium nitride is performed in an atmosphere of nitrogen, temperature of 700 to 900°C for 10 to 30 seconds by rapid thermal annealing.
- 9. The method in accordance with claim 1, wherein said interconnecting metal is aluminum or copper.
  - 10. The method in accordance with claim 9, wherein said

method further comprises a step of forming arc-thin film for preventing reflection by copper or aluminum before the patterning step of forming said metal interconnect.

- 11. The method in accordance with claim 10, wherein said arc-thin film is made of titanium.
  - 12. The method in accordance with claim 10, wherein said titanium nitride is formed by thermal decomposition of Tetradiethylaminotitanium at 300 to 450 °C.
    - 13. The method in accordance with claim 10, wherein said titanium nitride is formed by thermal decomposition of Tetradimethylaminotitanium at 300 to 450  $^{\circ}$ C.



## Amendments to the claims have been filed as follows

1. A method of forming a metal interconnect for a semiconductor device, comprising the steps of

forming a contact hole in an insulating layer formed on a semiconductor substrate;

depositing titanium and then titanium nitride layers, each having a predetermined thickness, on said insulating layer and in said contact hole by chemical vapor deposition;

thermally annealing said substrate in an atmosphere of nitrogen and/or helium, wherein said titanium nitride layer is phase-transformed to plural titanium nitride layers each of which layers has different nitrogen and/or helium content and a different phase state;

depositing a metal layer having low resistivity on the titanium nitride layer; and

patterning the layers formed on the contact hole and insulating layer.

- 2. The method in accordance with claim 1, wherein said titanium layer is formed by chemical vapor deposition which reacts TiCl<sub>4</sub> with NH<sub>3</sub>.
- 3. The method in accordance with claim 1, wherein said titanium nitride is formed by thermal decomposition of tetradimethylaminotitanium.
- 4. The method in accordance with claim 1, wherein said titanium nitride 25 is formed by thermal decomposition of tetradiethylaminotitanium.
  - 5. The method in accordance with claim 3 or 4, wherein said thermal decomposition is performed at a condition of temperature of 300 to 500°C, pressure of 5 to 10 mtorr.

5

15



- 6. The method in accordance with claim 1, wherein said thermal annealing of titanium nitride is performed in the atmosphere of nitrogen and/or helium, at a temperature of 400 to 600°C for 30 to 60 minutes.
- 7. The method in accordance with claim 1, wherein said thermal annealing of titanium nitride is performed in the atmosphere of nitrogen and/or helium, at a temperature of 700 to 900°C for 10 to 30 seconds by rapid thermal annealing.
- 8. The method in accordance with claim 1,3 or 4, wherein said metal layer is aluminum or copper.
  - 9. The method in accordance with claim 8, wherein said method further comprises a step of forming a thin antireflective coating (arc) film on said metal layer for preventing reflection of light from said metal layer before said patterning step.
  - 10. The method in accordance with claim 9, wherein said arc-thin film is made of titanium.





Application No: Claims searched:

GB 9604614.9

1-13

Examiner:

Peter Beddoe

Date of search:

18 April 1996

Patents Act 1977 Search Report under Section 17

#### Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): C7F (FHB,FHE,FHX,FACE,FACX,FAFE,FAHX,FAXE,FAXX); H1K

(KHAAB,KHABX,KHAAX,KHAD)

Int Cl (Ed.6): C23C (14/06,14/58,16/34,16/56); H01L 21/285

Other:

Online: WPI, CLAIMS

#### Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
х	EP 0525637 A1	(APPLIED) see esp col. 5 l. 50- col. 6 l. 32	1
x	EP 0514103 A1	(SGS) see esp col. 3 1. 2-30	. 1
х	EP 0209654 A2	(KABUSHIKI) see esp col. 3 1.10- col. 4 1. 51; col. 5 1. 19-26	1
x	US 5136362 A	(GRIEF) see esp col. 11 l. 45- col. 12 l. 38	1

- X Document indicating lack of novelty or inventive step
   Y Document indicating lack of inventive step if combined with one or more other documents of same category.
- & Member of the same patent family

- A Document indicating technological background and/or state of the art.
- P Document published on or after the declared priority date but before the filing date of this invention.
- E Petent document published on or after, but with priority date earlier than, the filing date of this application.